

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	171	((completion near3 (queue fifo buffer)) and ((event request work) near3 (queue fifo buffer))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 16:24
L2	836	((address near3 translation) and ((virtual logical) near3 (address id)) and (physical near3 (address id))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 16:25
L3	3	1 and 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 16:25

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L7	295	(("20060265525") or ("20070005815") or ("5655146") or ("20060265561") or ("4847748") or ("5377337") or ("5983341") or ("6226695") or ("6226695") or ("20060143506") or ("6163834") or ("20040193832") or ("5680425") or ("5802131") or ("5881303") or ("5958019") or ("6205507") or ("6874054") or ("20040123013") or ("20050165980") or ("20070078892") or ("20070168567") or ("20070239905") or ("20070050591") or ("5784550") or ("20050138161") or ("5892970") or ("5848283") or ("6321276") or ("6449283") or ("6760787") or ("20020007427") or ("5375215") or ("5625800") or ("6078983") or ("6092127") or ("6148394") or ("4410943") or ("4758949") or ("4805090") or ("4885683") or ("4937818") or ("4956771") or ("5016169") or ("5038280") or ("5513368") or ("5619408") or ("5634099") or ("5666494") or ("5701433") or ("5717587") or ("5784271") or ("5813038") or ("5822772") or ("5867728") or ("5897654") or ("5911065") or ("5938739") or ("5960459") or ("5978858") or ("6085261") or ("6088740") or ("6105080") or ("6128669") or ("6145042") or ("6160560") or ("6205506") or ("6219750") or ("6219750") or ("6253225") or ("6466326") or ("6477587") or ("6526485") or ("6671761") or ("6701386") or ("6754732") or ("7028151") or ("20020023186") or ("20040039877") or ("20050220128") or ("5894583") or ("4388489") or ("4441163") or ("4445176") or ("5339449") or ("5479615") or ("5504898") or ("5652914") or ("5671365") or ("5758190") or ("5854823") or ("5875343") or ("5875342") or ("5889944") or ("6016424") or ("6067643") or ("6070209") or ("6108741") or ("6115682") or ("6138192") or ("6459904") or ("6460124") or ("20040073622") or ("20050179944") or ("20060212607") or ("4272819") or ("5324025") or ("5926645") or ("6192461") or ("7073043") or	US-PGPUB; USPAT	OR	OFF	2007/11/20 12:30
11/20/07 2:57:19 PM C:\Documents and Settings\Nate\My Documents\EAST\workspaces\09819997.wsp						
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L8	499	(host near3 (adapter interface port connector)) and ((link network) near3 (adapter interface port connector)) and (packet near3 (switch engine processor)) and (address near3 translation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 12:58
L9	6250	(address near3 translation) and ((virtual logical) near3 (address id)) and (physical near3 (address id))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 13:02
L10	1930	(completion near3 (queue fifo buffer)) and ((event request work) near3 (queue fifo buffer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 13:06
L11	177	9 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 13:06
S27	1	((channel link) near3 (adapter interface port connector)) same (queue buffer) same (engine) same (cpu processor) same(address near3 translation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:34
S28	32	(host near3 adapter) with (address near3 translation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:35
S29	1844	709/250.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:59

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S30	9	COLLINS-BRIAN-M.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:59
S31	16	BERRY-FRANK-L.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:59
S32	7608	370/310,352,353,354.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 17:59
S33	498	(host near3 (adapter interface port connector)) and ((link network) near3 (adapter interface port connector)) and (packet near3 (switch engine processor)) and (address near3 translation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/20 12:58
S34	31	S32 and S33	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/19 18:15


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[E Lee](#)
[C Thekkath](#)
[D Dunning](#)
[P Druschel](#)
[G Regnier](#)
Efficient virtual interface architecture (VIA) support for the IBMSP switch-connected NT clusters - all 6 versions »

M Banikazemi, V Moorthy, L Herger, DK Panda, B ... - Parallel and Distributed Processing Symposium, 2000. IPDPS ..., 2000 - [ieeexplore.ieee.org](#)
 ... of this NIC is similar to the Micro Channel based SP2 adapter architecture reported in ... Therefore **virtual to physical address translation** is required. ...

Cited by 43 - [Related Articles](#) - [Web Search](#)

Two level address translation and memory registration system and method - all 4 versions »

DJ Garcia, DL Fowler - US Patent 6,163,834, 2000 - Google Patents
 ... **Translation/ Protection Table** 4KB minimum size 4KB aligned 8B entry ... Table Index MH

Memory Handle VA - **Virtual Address PSA** - **Pseudo Address PA** - **Physical ...**

Cited by 11 - [Related Articles](#) - [Web Search](#)

Decoupled hardware support for distributed shared memory - all 7 versions »

SK Reinhardt, RW Pfile, DA Wood - Proceedings of the 23rd annual international symposium on ..., 1996 - [portal.acm.org](#)

... tual **address translation** and fine-grain access control. **Virtual address translation** directs remote data accesses to local **physical memory**. ...

Cited by 70 - [Related Articles](#) - [Web Search](#)

Composite drive controller including composite disk driver for supporting composite drive accesses ... - all 3 versions »

CS Jones, A Davis - US Patent 5,548,783, 1996 - Google Patents

... the composite **address-to-physi- cal address translation**, the drive ... an Adaptec AHA-1540 host **adapter card** ... **virtual drive location** and sector **address informa- tion** ...

Cited by 39 - [Related Articles](#) - [Web Search](#)

System for accessing information in a data processing system - all 3 versions »

R Lary, R Willard, C Van Ingen, D Thiel, W Watson, ... - US Patent 5,386,524, 1995 - Google Patents

... mapping system generally comprises a **translation** 55 as a ... ROOT—PTR, may contain the

address of a mechanism ... software that enables the **adapter** to efficiently ...

Cited by 32 - [Related Articles](#) - [Web Search](#)

Realizing the performance potential of the virtual interface architecture - all 18 versions »

E Speight, H Abdel-Shafi, JK Bennett - Proceedings of the 13th international conference on ..., 1999 - [portal.acm.org](#)

... VI Architecture is designed to **address** three important ... region registered are provided to the VI **Adapter**. ... and avoid duplicate locking and **translation** operations ...

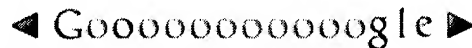
Cited by 71 - [Related Articles](#) - [Web Search](#)

... in hardware FIFO'S unused data start pointer to update virtual FIFO'S start address pointer for fast ... - all 3 versions »
DJ Lentz - US Patent 5,649,230, 1997 - Google Patents
... cessor and a peripheral processor. connected via the I/O bus 110 and bus adapter 120 and a bus ... corresponding to each virtual page. Address-translation reg- ...
[Cited by 20](#) - [Related Articles](#) - [Web Search](#)

InfiniBridge: an InfiniBand channel adapter with integrated switch - all 8 versions »
CR Eddington, M Technol, CA Santa Clara - Micro, IEEE, 2002 - [ieeexplore.ieee.org](#)
... InfiniBand host channel adapters deliver both virtual-to- physical address translation and memory ... HCA TCA Host channel adapter Target channel adapter ...
[Cited by 21](#) - [Related Articles](#) - [Web Search](#)

UTLB: a mechanism for address translation on network interfaces - all 10 versions »
Y Chen, A Bilas, SN Damianakis, C Dubnicki, K Li - ACM SIGOPS Operating Systems Review, 1998 - [portal.acm.org](#)
... An entry can either be invalid or contain the index in the translation table where the physical address for this virtual page is stored. ...
[Cited by 37](#) - [Related Articles](#) - [Web Search](#)

Design and implementation of a direct access file system (DAFS) kernel server for FreeBSD - all 7 versions »
K Magoutis - Proceedings of the BSD Conference 2002 on BSD Conference ..., 2002 - [portal.acm.org](#)
... memory NIC store virtual-to- physical address translations and ... buffer (TLB) to translate
virtual to physical ... sig- nifying whether the page translation is valid ...
[Cited by 31](#) - [Related Articles](#) - [Web Search](#)



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[\[PDF\]](#) [Extensibility safety and performance in the SPIN operating system - all 8 versions »](#)

BN Bershad, S Savage, P Pardyak, EG Sirer, ME ... - ACM SIGOPS Operating Systems Review, 1995 - cs.dartmouth.edu

... Extensible memory management Components **Physical storage -- physical address service**

Naming -- **virtual address service Translation -- translation service ...**

Cited by 872 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[Virtual address to physical address translation cache that supports multiple page sizes - all 3 versions »](#)

YA Khalidi, GR Anderson, SA Chessin, SI Kong, CE ... - US Patent 5,479,627, 1995 - Google Patents

... ment hardware such as a memory management unit (MMU) or paged memory management

unit (PMMU) performs the **address translation** from **virtual** addresses to **physical** ...

Cited by 61 - [Related Articles](#) - [Web Search](#)

[Translation buffer for virtual machines with address space match - all 4 versions »](#)

AH Mason, JS Hall, PT Robinson, RT Witek - US Patent 5,319,760, 1994 - Google Patents

... ad -dress, so whenever a **virtual address** is presented the ... management system finds the **physical address** by referencing ... are kept in a **translation buffer** within ...

Cited by 76 - [Related Articles](#) - [Web Search](#)

[Architectural support for translation table management in large address space machines - all 4 versions »](#)

J Huck, J Hays - Proceedings of the 20th annual international symposium on ..., 1993 - portal.acm.org

... Inverted Page Translation Table **Virtual Address Physical Address** PDIR VA I We PDIR Base ... Hashed Page Translation Table **Virtual Address** 1 1 J **Physical Address** ...

Cited by 92 - [Related Articles](#) - [Web Search](#)

[Shared virtual address translation unit for a multiprocessor system - all 3 versions »](#)

Y Fukunaga, T Bandoh, H Matsumoto, R Hiraoka, J ... - US Patent 4,481,573, 1984 - Google Patents

... which is used to look up the **translation table** to effect SV stem the **translation** to the **physical address**. Thirdly, a conventional job processor uses a **virtual** ...

Cited by 60 - [Related Articles](#) - [Web Search](#)

[The Quadrics network: high-performance clustering technology - all 56 versions »](#)

F Petrini, W Feng, A Hoisie, S Coll, E ... - Micro, IEEE, 2002 - ieeeexplore.ieee.org

... unit (MMU) translates 32-bit **virtual** addresses into ... To translate these **address- es**, the MMU contains a 16-entry, fully asso- ciative, **translation** look-aside ...

Cited by 245 - [Related Articles](#) - [Web Search](#)

Coherency for multiprocessor virtual address caches

JR Goodman - ACM SIGOPS Operating Systems Review, 1987 - portal.acm.org

... for large pages results in large **physical** memory, which ... in the cache indexed by **virtual**, rather than ... Since **address translation** is required only when a cache ...[Cited by 62](#) - [Related Articles](#) - [Web Search](#)**The Virtual Interface Architecture - all 6 versions »**

D Dunning, G Regnier, G McAlpine, D Cameron, B ... - Micro, IEEE, 1998 -

ieeexplore.ieee.org

... the memory. Nonvariable time for **virtual-to-physical address translation** is especially critical at the receiving endpoint. We did ...[Cited by 259](#) - [Related Articles](#) - [Web Search](#)**AN IN-CACHE ADDRESS TRANSLATION MECHANISM - all 3 versions »**

DA Wood, SJ Eggers, G Gibson, MD Hill, JM ... - portal.acm.org

... Many systems with **physical address** caches perform **address translation** in parallel with the cache access, deriving the index from the **virtual address** and the ...[Cited by 50](#) - [Related Articles](#) - [Web Search](#)**ATUM: A New Technique for Capturing Address Traces Using Microcode - all 3 versions »**

A Agarwal, RL Sites, M Horowitz - portal.acm.org

... be invaluable in studying the effects of **translation** lookaside buffer ... complete information for converting a **virtual-address** trace to a **physical-address** one. ...[Cited by 193](#) - [Related Articles](#) - [Web Search](#)

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[... hierarchical memories using a **virtual** storage scheme and **physical** to **virtual address translation** - all 4 versions »](#)

T Doi, T Takemoto, Y Nakatsuka - US Patent 5,526,509, 1996 - Google Patents

[... \[54\] METHOD AND APPARATUS FOR CONTROLLING ONE OR MORE HIERARCHICAL MEMORIES USING](#)

[A VIRTUAL STORAGE SCHEME AND PHYSICAL TO VIRTUAL ADDRESS TRANSLATION ...](#)

[Cited by 26](#) - [Related Articles](#) - [Web Search](#)

[Complete computer system simulation: the SimOS approach - all 10 versions »](#)

M Rosenblum, SA Herrod, E Witchel, A Gupta - Parallel & Distributed Technology: Systems & Applications, ..., 1995 - [ieeexplore.ieee.org](#)

[... Binary **translation** is useful for operating system studies as ... itself and for the private **address** spaces of ... each valid transla- tion between **virtual** and **physical** ...](#)

[Cited by 291](#) - [Related Articles](#) - [Web Search](#)

[The TLB slice—a low-cost high-speed **address translation** mechanism - all 2 versions »](#)

G Taylor, P Davies, M Farmwald - ACM SIGARCH Computer Architecture News, 1990 - [portal.acm.org](#)

[... Sun, SPUR\) avoids **address translation** altogether by using **virtual** tags. The other variant \(EL.XSI, I-11'\) accesses the 'l'LB and the **physical** cache tag ...](#)

[Cited by 40](#) - [Related Articles](#) - [Web Search](#)

[... memory system employing **virtual address** primary instruction and data **caches** and **physical address** ... - all 3 versions »](#)

GS Taylor, PM Farmwald, TP Layman, HX Ngo, AW ... - US Patent 5,542,062, 1996 - Google Patents

[... In such architectures, the cache is located after a **translation** lookaside buffer \(TLB\) has translated a **virtual address** into a **physical address**. ...](#)

[Cited by 39](#) - [Related Articles](#) - [Web Search](#)

[Software-Managed **Address Translation** - all 26 versions »](#)

B Jacob, T Mudge - Proc. HPCA-3, IEEE CS Press, 1997 - [doi.ieeecomputersociety.org](#)

[... systems could sus- tain long periods requiring no **address translation** at all ... the operating system is free to implement whatever **virtual-to-physical** mapping it ...](#)

[Cited by 53](#) - [Related Articles](#) - [Web Search](#)

[Architecture support for single **address** space operating systems - all 4 versions »](#)

EJ Koldinger, JS Chase, SJ Eggers - Proceedings of the fifth international conference on ..., 1992 - [portal.acm.org](#)

[... they define a unique mapping between **virtual** and **physical** addresses, they introduce a new constraint that ... and allows **address translation** to be removed from the ...](#)

[Cited by 70](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

Machine-independent virtual memory management for paged uniprocessor and multiprocessor architectures - all 58 versions »

R Rashid, A Tevanian Jr, M Young, D Golub, R Baron ... - Computers, IEEE Transactions on, 1988 - ieeexplore.ieee.org

... A. **Virtual Memory Data Structures** Four basic memory management ... or a user task, 3) the **address map**: a ... data structure (ie, a hardware-defined **physical address map** ...

Cited by 236 - [Related Articles](#) - [Web Search](#) - [Library Search](#)

Virtual storage dynamic address translation mechanism for multiple-sized pages - all 3 versions »

SW White - US Patent 5,058,003, 1991 - Google Patents

... tive words defines all of the pages in **physical** storage, ... The **virtual address translation** process consists of searching a chain. ...

Cited by 43 - [Related Articles](#) - [Web Search](#)

Address translator - all 3 versions »

H Ikegaya, H Umeno, T Kubo, Y Ukai, N Sugama - US Patent 4,802,084, 1989 - Google Patents

... a common segment, whereby that one of said **physical** addresses stored in said **address translation** buffer which corresponds to the **virtual address** specified by ...

Cited by 50 - [Related Articles](#) - [Web Search](#)

Dynamic flow instruction cache memory organized around trace segments independent of virtual address ... - all 3 versions »

A Peleg, U Weiser - US Patent 5,381,533, 1995 - Google Patents

... instruction requested by the execution unit is 35 not found in the cache memory (miss), the **physical address** or the **virtual address** after **translation** to physical ...

Cited by 138 - [Related Articles](#) - [Web Search](#)



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Virtual memory computer apparatus and address translation mechanism employing hashing scheme and ... - all 3 versions »

YA Khalidi, M Talluri, DG Williams, VP Joshi... - US Patent 5,446,854, 1995 - Google Patents
 ... such as a memory manage- 30 ment unit (MMU) or paged memory management unit (PMMU)

performs the **address translation** from **virtual** addresses to **physical** addresses ...

Cited by 31 - [Related Articles](#) - [Web Search](#)

Virtual to physical address translation scheme with granularity hint for identifying subsequent ... - all 3 versions »

RL Sites, RT Witek - US Patent 5,454,091, 1995 - Google Patents

... [45] DateofPatent: [54] **VIRTUAL TO PHYSICAL ADDRESS TRANSLATION SCHEME WITH**

GRANULARITY HINT FOR IDENTIFYING SUBSEQUENT PAGES TO BE ACCESSED ...

Cited by 22 - [Related Articles](#) - [Web Search](#)

Petal: distributed virtual disks - all 44 versions »

EK Lee, CA Thekkath - Proceedings of the seventh international conference on ..., 1996 - portal.acm.org

... The **virtual-to-physical address translation** module contains common routines used by the various data access and recovery modules. ...

Cited by 405 - [Related Articles](#) - [Web Search](#)

Virtual-address caches. Part 1: problems and solutions in uniprocessors - all 3 versions »

M Cekanov, M Dubois - Micro, IEEE, 1997 - ieeeexplore.ieee.org

... S/U RWX Page table Page table entry (PTE) Check rights RWX VMR ... RWX VMR ... Figure

1. **Virtual-to-physical address translation**. . Page 3. tual address. ...

Cited by 34 - [Related Articles](#) - [Web Search](#)

Method and apparatus for preloading different default address translation attributes - all 3 versions »

K Yamada, GN Hammond - US Patent 5,918,251, 1999 - Google Patents

... If the TLB 230 contains the **translation** for the **virtual address** 200, the **physical** page number is retrieved from the TLB 230 and concatenated with the m bits ...

Cited by 33 - [Related Articles](#) - [Web Search](#)

Method and apparatus for preloading default address translation attributes - all 3 versions »

GN Hammond - US Patent 5,918,250, 1999 - Google Patents

... If the **translation** corresponds to the **virtual address**, the **physical address** portion of the **translation** is concatenated with the offset portion of the **virtual** ...

Cited by 29 - [Related Articles](#) - [Web Search](#)

Content addressable memory having memory cells storing don't care states for address translation - all 3 versions »

EJ McLellan, BA Gieseke - US Patent 5,890,201, 1999 - Google Patents
... FIG. 1, there is shown a block diagram of a digital computer system that employs **virtual-to- physical address translation**. The digital ...
[Cited by 36](#) - [Related Articles](#) - [Web Search](#)

Eliminating the **address translation** bottleneck for **physical address** cache - all 2 versions »

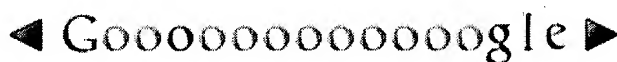
T Chiueh, RH Katz - ACM SIGPLAN Notices, 1992 - portal.acm.org
... of the most important factors in determining the processor cycle time is the placement and organization of the **virtual- to-physical address translation** hardware ...
[Cited by 23](#) - [Related Articles](#) - [Web Search](#)

UTLB: a mechanism for **address translation** on network interfaces - all 10 versions »

Y Chen, A Bilas, SN Damianakis, C Dubnicki, K Li - ACM SIGOPS Operating Systems Review, 1998 - portal.acm.org
... An entry can either be invalid or contain the index in the **translation** table where the **physical address** for this **virtual** page is stored. ...
[Cited by 37](#) - [Related Articles](#) - [Web Search](#)

Logically disconnectable **virtual-to-physical address translation** unit and method for such ... - all 3 versions »

DH Nguyen, RM Chu... - US Patent 5,564,052, 1996 - Google Patents
... [54] LOGICALLY DISCONNECTABLE **VIRTUAL-TO-PHYSICAL ADDRESS TRANSLATION UNIT AND METHOD FOR SUCH DISCONNECTION ... 10 / VIRTUAL*- PHYSICAL 201 ADDRESS TRANSLATION ...**
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The Virtual Interface Architecture - all 6 versions »

D Dunning, G Regnier, G McAlpine, D Cameron, B ... - Micro, IEEE, 1998 -
[ieeexplore.ieee.org](#)

... n consecutive entries in the **translation** and protection ... page size so that when the
virtual address cross-es ... the Intel Ether- Express Pro/100B network **adapter**. ...
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Experiences with a high-speed network adaptor: a software perspective - all 8 versions »

P Druschel, LL Peterson, BS Davie - Proceedings of the conference on Communications ...,
1994 - [portal.acm.org](#)

... data between main memory and network **adaptor**. ... Systems provide support for **virtual**
address DMA through ... hardware **virtual- to-physical translation** buffer (scatter ...
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Petal: distributed virtual disks - all 44 versions »

EK Lee, CA Thekkath - Proceedings of the seventh international conference on ..., 1996 -
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... global map is tried if an appropriate **translation** is not ... is to break up a **virtual**
disk's **address range** into ... strings using the Digital PMZAA-C host bus **adapter**. ...
[Cited by 405](#) - [Related Articles](#) - [Web Search](#)
Virtual display adapter - all 3 versions »

S Gupta, SP Larky, AW Peevers, JCS Clair - US Patent 5,113,180, 1992 - Google Patents

... **translation** mechanism within the **virtual display** Page 12. 5, 1 1 3, 1 80 **adapter**
810 translates the **address** and performs the graphics operation in the **physical** ...
[Cited by 25](#) - [Related Articles](#) - [Web Search](#)
MMMC-2: Efficient Support for Reliable, Connection-Oriented Communication - all 12 versions »

C Dubnicki, A Bilas, Y Chen, S Damianakis, K Li - Proc. of the Hot Interconnects Symposium
V, 1997 - [cs.unm.edu](#)

... The **address translation** (from **virtual** to **physical**) in the Myrinet VMCC implementation
uses a rmware-managed cache on the Myrinet network interface that ...
[Cited by 119](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)
Dynamic address translation system - all 2 versions »

Y Katsumata - US Patent 4,373,179, 1983 - Google Patents

... In the **virtual** memory system, the access protec -tion ... invention to realize a dynamic
address translation system for ... the channel or sub-system **adapter** for such ...
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